REMARKS

The Examiner's Final Action mailed on September 13, 2004 has been received and its contents carefully considered.

Claims 18-23 are pending in this application. Claims 18 and 23 are amended herein. Claim 18, as amended, remains the sole independent claim.

In the Final Action, the Examiner objects that Figures 2, 3(a) and 3(b) of the drawings should be designated by a legend such as -- Prior Art -- because only that which is old is illustrated. Replacement figures including a Prior Art legend are attached to this Amendment. Approval of the replacement figures and withdrawal of the objection are respectfully requested.

In the Final Action, claims 18, 19 and 22 are rejected under 35 USC 103(a) as being obvious over Heisley et al. (U.S. Patent No. 6,333,623) in view of the Applicant's admitted prior art. Claims 18, 19 and 22 are also rejected under 35 USC 103(a) as being anticipated by Kadanka (U.S. Patent No. 5,966,004) in view of the Applicant's admitted prior art. Claims 20, 21 and 23 are rejected under 35 USC 103(a) as being obvious over Kadanka in view of the Applicant's admitted prior art as applied to claim 18. In response, claims 18 and 23 are amended herein to more clearly distinguish the claimed invention over the applied references.

The Heisley reference discloses, in Figure 4, a voltage regulator (56) comprising a series type regulator (66 and 68) coupled to an output node (72) and supplied with a reference voltage (V_{REF}) and a first voltage (V_M) generated by dividing the voltage at the output node, and a shunt type regulator (62 and 64) coupled to the output node and supplied with the reference voltage and a second voltage the same as the first voltage from the divided voltage at the output node.

Similarly, the Kadanka reference discloses, in Figure 1, a voltage regulator (100) comprising a series type regulator (210 and 230) coupled to an output node (205) and supplied with a reference voltage (V_{REF}) and a first voltage generated by dividing the voltage at the output node, and a shunt type regulator (220 and 240) coupled to the output node and supplied with an off-set reference voltage and a second voltage the same as the first voltage from the divided voltage at the output node.

AMENDMENTS TO THE DRAWINGS

Please substitute the attached Replacement Sheets for Figures 1-4 of the drawings.

As amended, claim 18 is directed to a voltage regulator comprising "a series type regulator ... which is coupled to an output node, ... [having] a first transistor which is coupled between a first node and the output node ... and a shunt type regulator ... which is coupled to the output node, ... [having] a second transistor which is coupled between the output node and a second node". Claim 18 further recites that the shunt regulator includes "a constant current source which is coupled between the first node and the output node and which supplies a constant current to the output node." As noted on page 11, lines 9-13 of the specification, this feature advantageously prevents any analysis of the internal state of logic circuits connected as a load to the voltage regulator, by means of monitoring the power supply current waveform, as long as the load current does not exceed the capability of the constant current source.

By contrast, both Heisley and Kadanka fail to teach or suggest the recited constant current source. In Heisley, the variation of the current flowing through the pass element 68 follows directly the variation of the current flowing to the load through the output node V_{OUT}. Similarly, in Kadanka, the variation of the current flowing through the transistor 210 follows directly the variation of the current flowing to the load through the output node 205. Neither Heisley nor Kadanka employ "a constant current source which is coupled between the first node and the output node," as recited in claim 18, that provides the security feature discussed in the preceding paragraph.

In the Final Action, the Examiner acknowledges that the references fail to disclose the inclusion of a constant current source in the shunt regulator. To overcome this deficiency in the references, the Examiner points to prior art Figure 3(b) in the present application as illustrating that shunt regulators including a constant current source (B) were old and known in the art at the time of the invention. The Examiner argues that it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the voltage regulators of Heisley and Kadanka by including a constant current source in the shunt regulator in order to provide a smooth and consistent current to the load from the input power source as taught by the prior art.

The Applicant respectfully disagrees. In determining obviousness, the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. Hartness Int'l, Inc. v.

Simplimatic Eng'g Co., 819 F.2d 1100, 2 USPQ2d 1826 (FED. Cir. 1987). The Examiner must give adequate consideration to the particular problems and solution addressed by the claimed invention. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); In re Rothermel, 276 F.2d 393, 125 USPQ 328 (CCPA 1960). The fact that the prior art could be modified so as to result in the combination defined by the claims does not make the modification obvious unless the prior art suggests the desirability of the modification. In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

In the present case, neither Heisley nor Kadanka teach or suggest the combination of a series type regulator and shunt type regulator having a constant current circuit, which is claimed in the application. In Heisley and Kadanka, regulation of the voltage at the output node is achieved by using a combination of one transistor in series with the load and another transistor in shunt with the load. Neither employs a constant current circuit connected to the output node.

In the prior art section of the application, the series type regulator and the shunt type regulator, depicted in Figure 3(a) and 3(b) respectively, are discussed as alternative implementations for the voltage regulator 3 shown in Figure 2. The rationale for the claimed combination is explained elsewhere, in the detailed description section of the application at page 11, lines 9-21. The rationale is to obtain the data security benefits of using a shunt type regulator with a constant current circuit, while limiting power consumption when load current is high by combining the shunt type regulator with a series type regulator. There appears to be nothing in the Heisley and Kadanka references and the Applicant's admitted prior art, to suggest to one of ordinary skill in the art the benefits and desirability of the claimed combination.

Accordingly, it is respectfully submitted that amended claim 18, as well as claims 19-23, patentably distinguish over both of the applied prior art references. Further, it is believed that the amendment herein to claim 23 renders the Examiner's rejection of that claim moot.

In summary, it is submitted that this Amendment places the application in condition for allowance. Notice of allowance and the passing of this application to issue, are earnestly solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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Date

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Attachment:
- Replacement Drawing Sheets (Figs. 1-4)